

Remarks

In the Office Action dated November 18, 2005, claims 13, and 15-19 were objected to for various informalities which have been corrected.

Claims 1-3, 5-8, 10, 12, 13, 15, and 20 were rejected as being obvious over U.S. patent 5,871,562 to Chang et al. in view of U.S. Patent 6,162,737 to Weimer et al. and further in view of U.S. Patent 5,565,384 to Havemann. Claims 4, 9, and 11 were rejected as being obvious over Chang et al. in view of Weimer et al. and Havemann and further in view of U.S. Patent 6,730,570 to Shin et al. (erroneously identified as 2004/011377A1 on page 6 of the Office Action). Finally, claims 16-19 were rejected as being obvious over Chang et al. in view of Weimer et al. and Havemann and further in view of published U.S. Patent Application 2002/0064968 to Kim et al.

In response, applicants have canceled claims 4 and 11, amended claims 1, 13, and 15-18, and added new claims 21. Claims 1-3, 5-10, and 12-21 are pending for consideration.

At the threshold of this response, applicants generally object to the piecemeal mosaic rejections postulated by the Office Action. It seems that no number of marginally related (or entirely unrelated) documents is too many for the examiner to crop through their exhaustive descriptions of various "semiconductor" devices seeking some incidence of application for one or more steps used in the subject invention. Thus, any use of polysilicon, any use of BPSG, any use of a buffer layer, and any use of a wet or dry etching method is sufficient to render obvious some portion of the claimed subject matter. The Office Action makes little if any attempt to even suggest a basis in the prior art for proposed combination of references. Evidentially, in the mind of the examiner, any use of a particular step within the fabrication of a semiconductor device is sufficient to substantiate its inclusion within an obviousness rejection of any other semiconductor device – overall structure, purpose, and fabrication limitations notwithstanding.

This having been said, applicants submit that even accepting the remarkable proposed combination of references at face value, no legitimate art rejection has been postulated for the subject matter of original claim 4. Of note original claim 4 has been canceled and independent claim 1 amended to incorporate the subject matter of original claim 4.

In particular, Shin et al is not a reference upon which the examiner may rely in postulating a rejection of the ending claims. The effective U.S. filing date of Shin et al is January 22, 2003 while the subject application properly claims foreign priority back to an effective U.S. filing date of November 22, 2002. Thus, Shin et al can not form the basis of the postulated rejection of claims 4, 9, and 11.

The importance of the high-density plasma CVD nature of the silicon oxide film used to form the recited first interlayer insulating film is explained on pages 6 and 7 of the subject specification. Absent Shin et al., the art of record fails to suggest or disclose this particular feature of amended claim 1. Hence, claims 1-3, 5-10, and 12-20 are allowable over the art of record.

Similarly, the art of record fails to suggest or disclose, as recited in new claim 21, the steps of:


- forming a buffer layer over the source region, the drain region and the sidewall spacers of the gate;
- forming an etch stop layer on the buffer layer to obtain an intermediate structure;
- forming a first interlayer insulating film over the intermediate structure, wherein the first interlayer insulating film has an etching rate slower than the etching rate of the buffer layer relative to a defined dry etching process;

Thus, new claim 21 is also allowable over the art of record.

Allowance of the pending claims is respectfully requested.

Respectfully submitted,

Volentine Francos & Whitt, P.L.L.C.



Stephen R. Whitt
Registration No. 34,753

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Volentine Francos & Whitt, PLLC
One Freedom Square
11951 Freedom Drive, Suite 1260
Reston VA 20190
Tel. No. 571-283-0720
Fax No. 571-283-0740